A Wireless Sensor-Brain Interface System for Tracking and Guiding Animal Behaviors Through Goal-Directed Closed-loop Neuromodulation

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Abstract

This paper presents a wireless sensor-brain interface (SBI) system featuring a linked bidirectional neural interface IC and an image sensor IC for animal tracking. The system enables a novel experiment in which swimming rats navigate a water maze guided solely by brain stimulation. Closed-loop mapping of extracted rat behaviors to stimulation parameters is implemented with novel hardware acceleration for real-time operation with short latency. The neural interface device integrates stimulators with a new charge-balancing design and neural recording front-ends with stimulation artifacts rejection. A low-power UWB link is designed for wireless communication. The system has been successfully validated in multiple rats. **Keywords:** neural interface, closed-loop neuromodulation

Introduction

Sensory feedback is essential for controlling motor functions. Prostheses to restore movement after injuries, such as amputation or stroke, similarly use sensory feedback to improve performance. This feedback can be provided by SBI, which links the output of a peripheral sensor on the prosthesis to modulated stimulation of the nervous system. New SBI paradigms are often tested in animals, such as by directing rats through mazes with brain stimulation [1-4]. To test the limits of artificial sensory encoding, more challenging SBI paradigms with greater degrees of freedom are needed. Thus, we designed a wireless system for water maze experiments, in which swimming rats seek a randomly placed, submerged platform using only brain stimulation (Fig. 1). This new design supports more versatile and advanced experimental paradigms than prior arts (including our previous design [3]) and permits the study on how animals actively adapt behaviors to artificial sensory feedback [4].

System Architecture

The system consists of a neural interface device and a host (Fig. 1). The neural interface device includes an implantable part and a wearable part, wirelessly linked with no through-skin connectors. Electrodes are chronically implanted in the sensory cortex and routed to the implantable part under the skin. The implantable IC integrates 10-channel programmable stimulators with a novel charge balancing design, 16-channel neural amplifiers with stimulation artifacts rejection, and a 12-bit SAR ADC for digitizing neural signals and electrode impedance. The wearable part communicates with the host through a UWB link and relays information from and to the implantable part through an inductive link, which is also used for powering the implantable part to permit a battery-free implant.

The host consists of an image sensor IC with on-chip object detection, a UWB transceiver, and an FPGA to accelerate animal tracking and closed-loop stimulation mapping algorithms. During the water maze experiment, the image sensor is used with a wide-angle lens and placed above the water tank. A red optical filter is added to the lens, and the wearable part of the device is dyed red to facilitate tracking. Animal behavioral markers are extracted at 100 frames/s (i.e., <10ms delay) and mapped to stimulation parameters with flexible configuration.

Circuits Implementation

Key circuit design innovations are highlighted below. Minimizing residual charge is critical for the safety of long-term electrical stimulation [5]. Charge-balanced biphasic stimulation (in which a reversal phase follows the stimulation phase) is commonly adopted, and a discharge phase is often added to remove any residual charge [6]. However, the discharging time constant has poor controllability, making it not suitable for the highly frequent stimulation needed in SBI. Here, we developed a stimulator that terminates the reversal phase when a net-zero charge condition is met (Fig. 2). A switched capacitor circuit samples the initial stimulation compliance voltage and sets the condition for terminating the reversal phase accordingly (Fig. 3). The design has been validated in vivo and successfully avoids charge accumulation. Stimulation artifacts may saturate neural amplifiers and block neural responses. We designed a circuit that temporarily elevates the amplifier's high-pass frequency corner f_{HP} during stimulation (Fig. 4). This is done by tuning the feedback pseudo resistor using a voltage generated by a shared DAC. The design has also been validated in vivo.

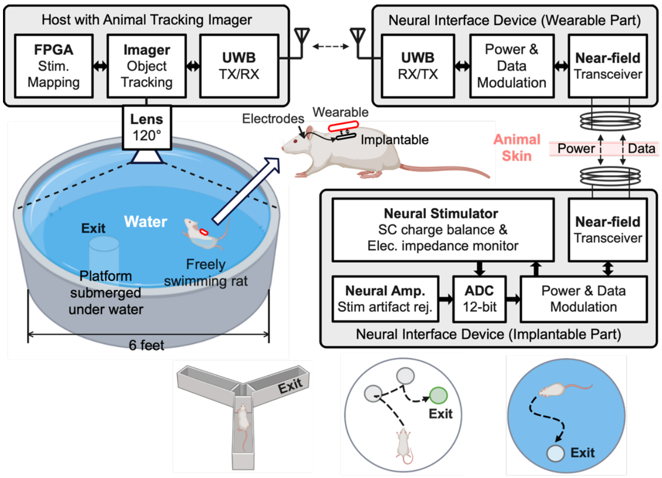
The image sensor consists of 160×160 digital pixels. Each pixel generates row- and column-level event signals when the voltage of the photodiode crosses a threshold. A global shutter latches the row and column events, which are processed by on-chip 1-D convolutional filters to determine the center coordinates of the object (Fig. 5). Coordinates in consecutive frames are used to estimate three markers: animal speed, distance to exit, and swimming deviation angle. The Euclidean distance calculation is simplified by an approximation function implemented by a custom accelerator module in FPGA. The arccosine function used for angle calculation is implemented by a LUT. Extracted markers are mapped to stimulation magnitude and frequency by a 2×3 matrix and a bias vector, implemented by a matrix-vector multiplication (MVM) accelerator.

Experimental Results

Both chips are fabricated in a 180 nm CMOS process (Fig. 8). The measured power of the implantable part is 93 µW, and the size is 20×9 mm^2. The input referred noise of the neural amplifier is 4.7 µV (1 Hz to 1kHz). The gain is programmable up to 60 dB and the CMRR is 103 dB. The ENOB of the ADC is 11.2 at 100 kSps (Fig. 4). The AUC of the detected region is 96.7% and the standard deviation of the coordination error is 2.7% (over 1M frames tested). The UWB transceivers achieved a BER of 10^{-5} at a 3 m distance with 9.7 pJ/bit for TX and 131 pJ/bit for RX (Fig. 6). The rats reliably learned to swim to the submerged platform with SBI feedback as efficiently as to an un-submerged platform with natural vision (Fig. 7). The table in Fig. 8 summarizes the key parameters of the design compared to the prior art. This unique system can enable paradigm-shifting neuroscience studies and neuroprosthetic applications.

References

[1] X. Wu, *Nat. Biomed. Eng.*, 2022. [2] S.L. Coffin, *Neuron*, 2022. [3] X. Liu, *ISCAS*, 2017. [4] A.G. Richardson, *PNAS*, 2019. [5] U. Shin, *ISSCC*, 2022. [6] Y. Jia, *ISSCC*, 2020.



	Y-Maze [1]	Barnes Maze [2]	Watermaze (This work)
Animal Motivation	Reward	Reward	Natural + Reward
Degree of Freedom	Low	Moderate	High
Sensory Feedback	Binary	Simple	Advanced
Learning Process	Passive	Passive	Active

Fig. 1 Overview of the system and comparison with other paradigms.

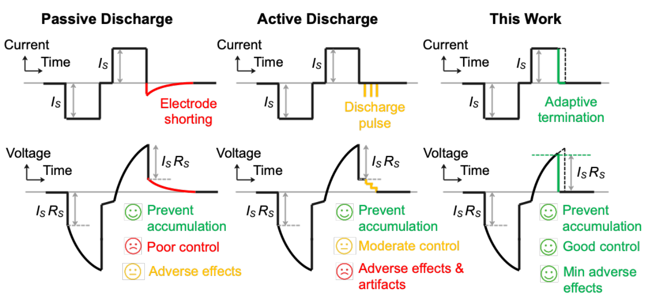


Fig. 2 Proposed stimulation scheme with adaptive termination

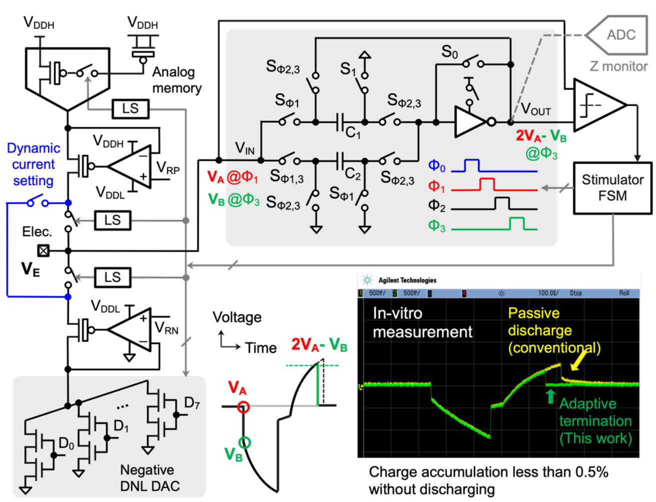


Fig. 3 Circuit implementation of the stimulator and measurement

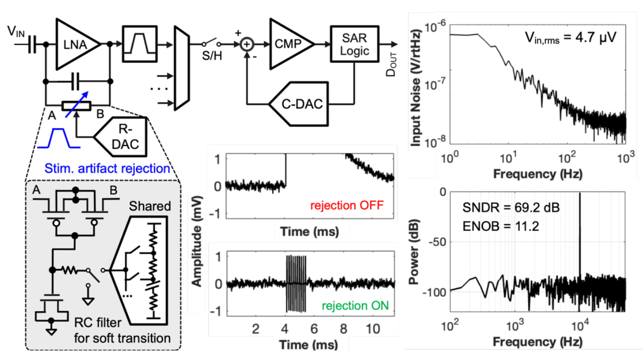


Fig. 4 Neural front-end and ADC with stimulation artifact rejection

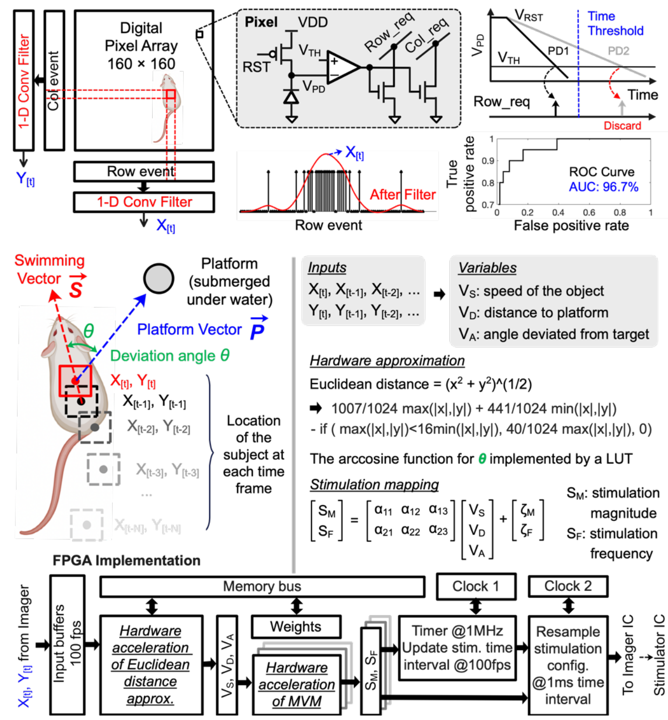


Fig. 5 Image sensor with object tracking and stimulation modulation

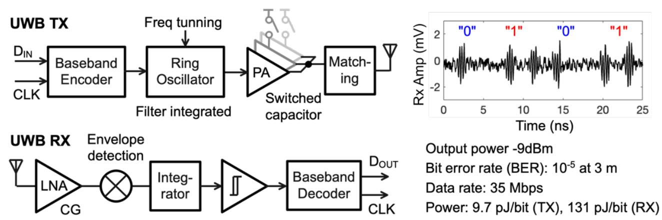


Fig. 6 UWB transceiver and measured key performance

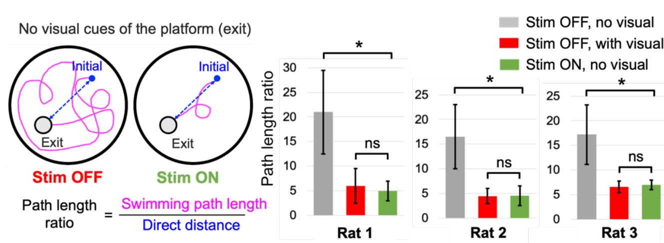
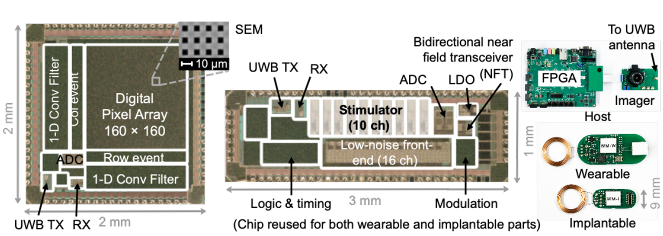


Fig. 7 Water maze experimental results in three rats



Publication	ISSCC '20 [7]	ISSCC '20 [6]	VLSI '21 [8]	VLSI '21 [9]	ISSCC '22 [5]	This work
Technology	180 nm	350 nm	65 nm	65 nm	65 nm	180 nm (2 ICs)
Supply voltage	1.5 V	1.8/3.3/4 V	2.5 V	0.4/1 V	1.2 V	1.8/3.3/5 V
Stim. (max. current)	2 ch (12 mA)	4 ch (0.78 mA)	1024 (0.6 mA)	1 ch (1mA)*	16 ch	10 ch (0.25mA)
Q balancing	unknown	Active/passive	Single I-source	unknown	Active	Adaptive
Rec. (noise)	8 ch (1.7 µV)	16 ch (3.46µV)	1024 (8.98 µV)	1 ch (N/A)*	256 ch (3.2 µV)	16 ch (4.7 µV)
Stim. artifact rej.	Yes	Yes	—	—	—	Pole shifting
Vision Sensor	—	—	—	—	—	160 x 160 DPS
Closed-loop (CL) op.	Yes	—	—	—	NeuralTree	Sensory Feedback
CL Latency	0.3 s	—	—	—	< 1 s	0.01 s
Wireless Data	—	RF	—	OOk 10Mbps	—	UWB 35Mbps
Wireless Pwr.	—	Inductive	—	Yes	—	Inductive
In-vivo Exp.	Yes	Yes	Yes	Yes	—	Water maze

* Channel count not explicitly specified in the paper, estimated based on the figure

Additional references: [7] Y. Wang, *ISSCC*, 2020 [8] D. Yoon, *VLSI*, 2021 [9] B. Chatterjee, *VLSI*, 2021

Fig. 8 Chip micrograph, device prototypes, and benchmarking table